ABSTRACT

[1092] A digital PLL includes an adaptive PFD, an adaptive loop filter, an iDAC, an ICO, and a divider. The adaptive PFD receives a reference signal and a feedback signal, determines phase error between the two signals, and provides a PFD value for each phase comparison period. The magnitude of the PFD value is adjusted to achieve fast frequency acquisition and reduced jitter. The adaptive loop filter updates its output whenever a PFD value is received, widens the PLL loop bandwidth if a large phase error is detected, and narrows the loop bandwidth if a small average phase error is detected. The iDAC, which can be implemented with both steered and single-ended current sources, converts the loop filter output into analog current. The ICO provides an oscillator signal having a phase determined by the iDAC output. The divider divides the oscillator signal by a factor of N and provides the feedback signal.